Textile & Leather Review

ISSN 2623-6281 | www.tlr-journal.com | 10.31881/TLR

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How to cite: Li Q. Design and Implementation of a Multi-Layer Stacked Miniaturized High-Voltage Pulse Generator. Textile & Leather Review. 2026; 9:2870-2891.
https://doi.org/10.31881/TLR.2026.2870

How to link: https://doi.org/10.31881/TLR.2026.2870

Published: 25 April 2026

Design and Implementation of a Multi-Layer Stacked Miniaturized High-Voltage Pulse Generator

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Article
https://doi.org/10.31881/TLR.2026.2870
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ABSTRACT

The miniaturization of high-voltage pulse generators is critical for emerging portable and integrated applications, particularly in the advanced electro-physical processing of textiles and leather. Traditional planar printed circuit board (PCB) designs face fundamental limitations in size and parasitic performance. This work presents the design, fabrication, and experimental validation of an ultra-compact, multi-layer stacked solid-state high-voltage pulse generator. The module integrates a flyback boost converter using a low-temperature co-fired ceramic (LTCC) transformer, an energy storage capacitor, and a MOS-controlled thyristor (MCT) switch within a 15.0×15.0×15.7 mm³ volume. A vertical stacking architecture separates low-voltage control from high-voltage discharge layers, minimizing the commutation loop. Electrostatic simulations confirm insulation integrity at 1.2 kV, while electromagnetic extraction shows a total loop inductance of 45.35 nH. Experimental results demonstrate a steady boost to 1.18 kV and a peak discharge current of 2.016 kA with an underdamped oscillatory waveform. The prototype validates the multi-layer stacking methodology as a viable path toward high-density, integrated pulsed power systems tailored for modern, compact material treatment equipment.

KEYWORDS

multi-layer stacking, solid-state pulse generator, high-voltage miniaturization

INTRODUCTION

High-voltage pulse generators are used in a variety of emerging applications and are playing an increasingly vital role in the advanced processing of textiles and leathers. For example, they are crucial for generating non-thermal micro-plasmas, which is an eco-friendly way to modify the surface of heat-sensitive textiles and leathers without affecting their overall properties.[1] Furthermore, electric pulse processing is widely used in the physical and mechanical treatment of natural fibres, such as cottonising hemp, to control their structural characteristics and ensure optimal spinning capabilities.[2] Alongside other versatile applications

like biomedical electroporation[3,4] and localized discharge testing[5,6], these advanced material treatments are progressively shifting towards flexible, small-scale manufacturing and in-field deployment. As these applications increasingly shift towards point-of-care and in-field deployment, there is a growing demand for the miniaturization and high-density integration of pulsed power systems.[5,7] However, traditional high-voltage pulse generators, such as those based on Marx topologies or pulse-forming networks (PFNs), rely on bulky components and large spatial isolation to prevent dielectric breakdown.[3,8] This inherent limitation significantly restricts their portability.

Miniaturizing high-voltage pulse generators is a key area of research, driven by the growing demand for compact, portable and integrated systems in various applications.[9] Recent research has focused on overcoming the limitations of these systems through a multi-pronged strategy.[10,11] One significant trend is the shift from conventional spark gaps to robust, all-solid-state switching architectures that leverage the superior performance of devices such as silicon carbide (SiC), metal–oxide–semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs).[12] These solid-state switches offer reliability, jitter control and, crucially, the potential for monolithic integration.[13] Concurrently, innovations in passive component technology are being actively pursued.[14] This includes developing compact, high-energy-density dielectric materials for pulse forming networks, such as advanced polymer films and antiferroelectric capacitors.[15,16] However, the majority of extant solid-state miniature pulse generators employ planar printed circuit board (PCB) layouts.[12,17,18] In a planar architecture, achieving high voltage necessitates substantial creepage distances and electrical clearances, which, in turn, increases the overall footprint.[19,20] Furthermore, the extended trace lengths in planar designs introduce significant parasitic stray inductance. During periods of high di/dt and dv/dt switching transients, these parasitic parameters induce waveform ringing, voltage overshoots, and compromised pulse rise times, thereby degrading the overall system performance.[21,22]

In order to overcome the spatial and parasitic bottlenecks inherent in planar designs, three-dimensional (3D) integration and multi-layer stacking technologies have emerged as promising solutions. The vertical dimension is utilized in 3D stacking, resulting in increased power density and reduced commutation loop. However, the compact integration of a flyback boost converter, high-voltage energy storage capacitors, and solid-state switches poses significant challenges related to high-voltage insulation.

The present paper puts forward a proposal for an ultra-compact, multi-layer stacked solid-state high-voltage pulse generator, which has been implemented within a small footprint of just $15 \times 15 \times 15.7\,\mathrm{mm}^3$. The

integrated module consists of a miniature flyback boost circuit, a high-voltage energy storage capacitor, and a high-voltage solid-state switch.

The remainder of this paper is organized as follows: Section II provides a comprehensive account of the circuit architecture and the selection of components. Section III describes the multi-layer stacking method and the three-dimensional integrated structure. Section IV presents the results of three-dimensional electromagnetic simulations, with a focus on insulation verification and the extraction of parasitic parameters. Section V introduces the experimental setup, performance evaluation results, and comparisons with other compact designs. Finally, Section VI concludes the paper.

CIRCUIT ARCHITECTURE AND DESIGN

System Overview

The proposed miniaturized high-voltage pulse generator schematic is illustrated in Figure 1. In order to achieve high-density integration within the strict volumetric constraint, the system architecture is designed with a minimalist yet highly efficient topology. The process is divided into two primary stages.

1) Flyback HV Converter: The primary function of this stage is to step up the low-voltage DC input (denoted as VIN+ and VIN-) to the target high-voltage level required for pulse generation. The stage under consideration comprises a primary-side solid-state switch, a micro high-frequency step-up transformer, and a high-voltage rectifying diode. The flyback switch is driven by an external pulse-width modulation (PWM) signal. During the ON-state of the flyback switch, the primary winding conducts, and energy is stored in the magnetizing inductance of the transformer core. It is evident that, in accordance with the dot convention, the transformer windings exhibit an opposing polarity. Consequently, the secondary-side rectifying diode is reverse-biased, thereby isolating the load. It is evident that when the flyback switch is deactivated, the collapsing magnetic field induces a high voltage across the secondary winding. The diode becomes forward-biased, thereby transferring the stored magnetic energy to the storage capacitor.
2) Pulse Discharge Circuit: This stage functions as both the energy buffer and the pulse generator loop. The system under discussion comprises a high-voltage energy storage capacitor and a solid-state pulse switch. The energy storage capacitor functions as a localized charge reservoir, accumulating energy in a sequential manner from the flyback converter until the target peak voltage is attained. The solid-state pulse switch remains in the blocking state during the charging phase. Once an external triggering pulse is applied to its control terminals (TRIGGER+ and TRIGGER-), the pulse switch rapidly transitions into the conduction

state. This transition establishes a low-impedance discharge loop, thereby instantaneously releasing the electrical energy stored in the capacitor to the Pulse Output terminals. This, in turn, results in the generation of a high-voltage pulse across the external load.

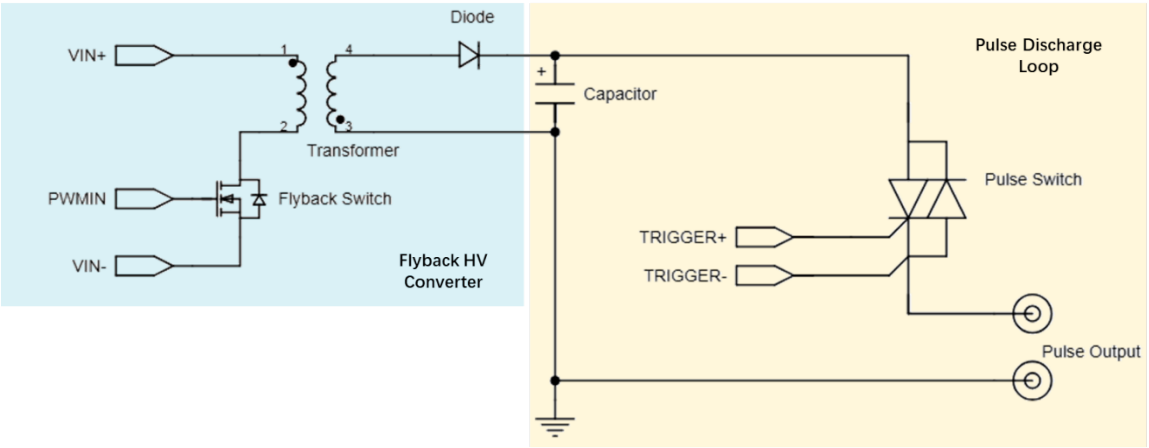

Figure 1. Overall circuit schematic of the proposed miniaturized high-voltage pulse generator, comprising a flyback boost converter and a solid-state pulse discharge loop

The architecture of the system is two-stage, with the low-voltage charging control isolated from the high-voltage discharge loop. This ensures stable energy conversion. In order to accommodate these two functional components within the target volume, the selection of surface-mount devices and a customized multi-layer stacking strategy are imperative. These topics will be addressed in greater detail in the ensuing sections.

Component Selection and Auxiliary Circuit Design

In order to satisfy the rigorous volumetric requirements of the module whilst maintaining optimal pulsed power performance, it is essential to meticulously select the critical components and to devise a sophisticated control loop design.

For the localized energy storage module, an anti-ferroelectric (AFE) capacitor (220 nF, 1200 V) is selected, as illustrated in Figure 2(a). AFE dielectric materials exhibit a unique electric-field-induced phase transition, offering significantly higher energy storage density and faster charge-discharge rates compared to conventional linear ceramics. The device's compact footprint, measuring 10.5 × 11.0 × 5 mm, is well-suited to the proposed multi-layer stacking architecture.

For the high-voltage step-up stage, a Low-Temperature Co-fired Ceramic (LTCC) integrated chip transformer is utilized, as illustrated in Figure 2(b). The four-port surface-mount magnetic component under consideration

provides a 1:8 turns ratio. The transformer's utilization of LTCC technology results in the elimination of the bulkiness of traditional wire-wound magnetic cores, thereby achieving a substantial reduction in the planar footprint and vertical profile.

The core of the pulse discharge loop is the solid-state trigger switch, for which a MOS-Controlled Thyristor (MCT) is employed [see Fig. 2(c)]. An MCT is a sophisticated power semiconductor device that combines the low on-state conduction loss and substantial surge-current capability of a thyristor with the high-input-impedance, voltage-controlled gate characteristics of a MOSFET. The selected MCT has dimensions of 6 × 8 × 1.5 mm and is capable of withstanding a maximum peak discharge current of 4 kA. Additionally, the device integrates an anti-parallel freewheeling diode, which effectively protects the switch from reverse voltage transients during underdamped oscillatory discharge phases.

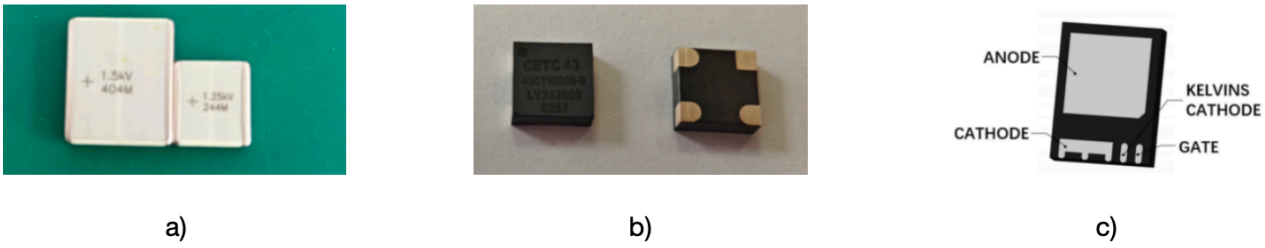

Figure 2. Key components of the miniaturized solid-state pulse generator: (a) 1200V, 220nF anti-ferroelectric (AFE) energy storage capacitor on the right, compared with a ; (b) LTCC integrated chip high-voltage transformer with a 1:8 turns ratio; (c) ultra-compact MOS-controlled thyristor (MCT) with a built-in anti-parallel freewheeling diode

The requirement for miniaturization has led to the design of a custom LTCC transformer that does not incorporate an auxiliary winding or center tap. This precludes the use of conventional primary-side regulation. Consequently, a direct high-voltage sampling feedback mechanism coupled with pulse skipping modulation (PSM) is implemented to regulate the flyback boost process.

As demonstrated in Figure 3, the output DC voltage is subject to continuous monitoring through the utilization of a high-voltage resistive divider network. The attenuated voltage signal is then introduced into a voltage comparator, which evaluates it against a predefined low-voltage reference threshold. The output logic of the comparator is then processed by a differential gate driver to modulate the primary-side flyback switch. Upon attaining the designated high voltage target, the comparator instigates the PSM controller to bypass the incoming PWM pulses, thereby effecting a temporary cessation of the boost process. In the event of a voltage

drop below the threshold, whether due to leakage or a pulse discharge event, the PWM pulses are re-enabled. This PSM strategy maintains the target high voltage with minimal static power consumption, ensuring voltage regulation without the need for auxiliary magnetic structures.

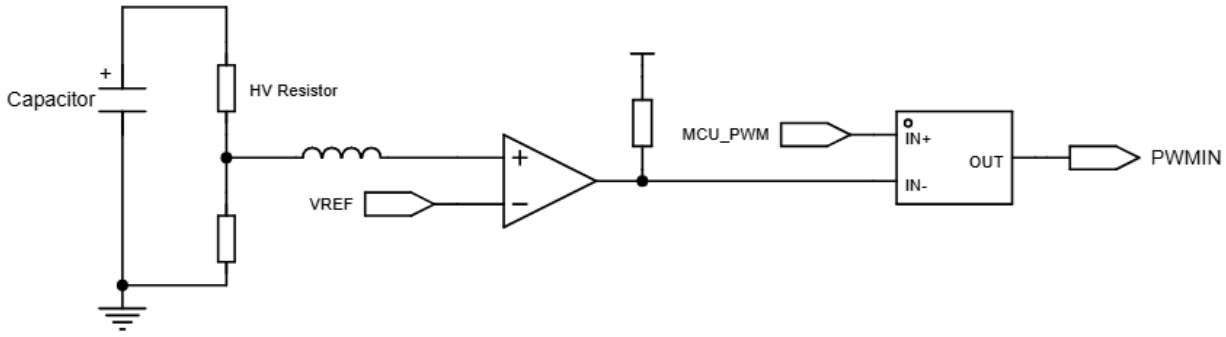

Figure 3. Schematic diagram of the high-voltage sampling feedback and auxiliary control circuit based on pulse skipping modulation

MULTI-LAYER STACKING AND INTEGRATION STRUCTURE

In order to facilitate the realization of the highly integrated solid-state pulse generator within the strict volumetric limit of approximately $15 \times 15 \times 15.7\,\mathrm{mm}^3$, a customized multi-layer stacking architecture is proposed. In contrast to conventional planar printed circuit board (PCB) designs, which necessitate substantial planar creepage distances for high-voltage insulation, the proposed vertical stacking strategy employs the Z-axis space in an efficient manner. The configuration of the stacked structure is illustrated in Figure 4. The system is structurally divided into six functional layers (designated A to F from top to bottom) to ensure the isolation of low-voltage control circuitry from the high-voltage discharge loop, whilst minimizing parasitic inductance.

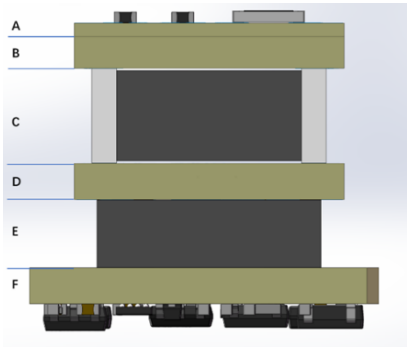

Figure 4. Cross-sectional view of the multi-layer integrated structure of the pulse generator, illustrating the vertical stacking configuration from Layer A to Layer F

The specific materials, functional components, and geometric dimensions for each layer are detailed in Table 1. The dimensions of the module are determined by the length and width of the bottom baseboard (Layer F). The height is calculated by adding the heights of the individual plates, resulting in 15 × 15 × 1.57 mm^3.

Table 1. Material and Component Allocation of the Multi-Layer Stacked Structure

Layer	Substrate/Material	Main Components	Dimensions (L×W×H, mm)
A	FR4	Load output terminal, High-voltage sampling network	12×12×1.2*
B	FR4	Framework with embedded MCT chip	12×12×1.6
C	Capacitor	Energy storage capacitor	10.5×11.0×5.0
D	FR4	Embedded high-voltage rectifying diode	12×12×1.6
E	LTCC transformer	Step-up high-voltage transformer	9×9×3.0
F	FR4	Control circuit, PWM & gate drivers	15×15×2.6*

- The heights for Layer A and Layer F include the thickness of surface-mounted components.

The vertical arrangement of layers A through F is governed by an electrical potential hierarchy, whereby low-voltage generation occurs at the bottom layer and high-voltage discharge takes place at the uppermost layer. Layer F receives external control signals (PWMIN, TRIGGER+ and TRIGGER-) that are utilized for the management of energy storage and pulse output processes. Additionally, Layer F receives a low-voltage power supply input (VIN+ and VIN-), which is typically 12 V DC. The components on Layer F encompass the PSM control circuit and differential gate drivers, which facilitate the conversion of the external 3.3 V signal into the control signals required by the transformer and MCT. The transformer, which is of the compact LTCC variety, is located in Layer E. This transformer is of critical importance as it serves to increase the voltage. As illustrated above,

Layer D contains the embedded rectifying diode, which functions to effectively block reverse high voltage from affecting the primary side.

The core energy buffer, the capacitor (Layer C), occupies the physical center of the stack. Layer B incorporates an FR4 framework with the MCT chip integrated within it, thereby positioning the solid-state switch near the energy storage capacitor.

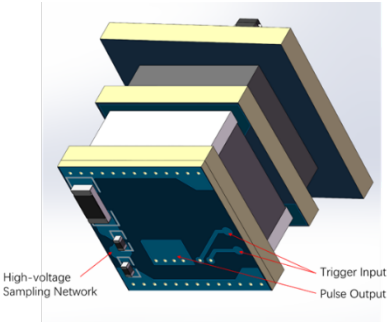

Figure 5. Detailed view of the top interface (Layer A), showing the annotated high-voltage sampling resistor network, the trigger input terminals, and the pulse output interface

In conclusion, Layer A constitutes the uppermost interface of the entire module, as illustrated in Figure 5. This layer is composed of the load output terminals and the localized high-voltage sampling resistor network. As illustrated in Figure 5, the high-voltage sampling network is implemented using surface-mount resistors, thereby providing precise feedback for the PSM control loop on Layer F. The top layer is also equipped with dedicated trigger input terminals, which facilitate interface with the pulse triggering signal.

This specific layer allocation offers two key advantages: maximizing the physical distance between sensitive low-voltage logic (Layer F) and high-voltage output (Layer A), and positioning the MCT switch (Layer B) between the storage capacitor (Layer C) and the output terminal (Layer A) to minimize the primary high-voltage commutation loop's length, thereby suppressing parasitic inductance and achieving a fast rise time.

ELECTROMAGNETIC SIMULATION AND ANALYSIS

Electric Field Distribution

In order to verify the insulation reliability and structural integrity of the stacked architecture under high-voltage stress, an electrostatic simulation was performed using CST Studio Suite. Due to the multi-layer module's limited spatial dimensions, there is a notable proximity between the high-voltage traces and low-voltage control layers. This raises potential concerns regarding dielectric breakdown.

To evaluate this, a 3D geometric model of the critical sub-assembly within the stacked structure was constructed in the simulation environment, as illustrated in Figure 6. This model captures the spatial arrangement of the FR4 substrates, the metallic interconnecting vias, and the geometric boundaries of the components.

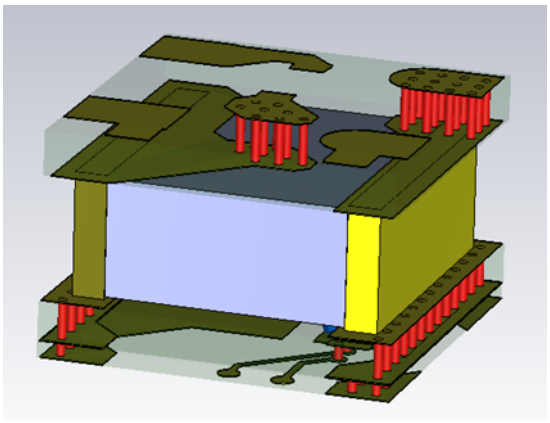

Figure 6. 3D geometric model of the multi-layer stacked sub-assembly constructed in CST Studio Suite

The simulation was designed to emulate the worst-case static electrical stress occurring at the conclusion of the boost phase, precisely when the capacitor is fully charged. As illustrated in Figure 7, a constant DC excitation voltage of 1200 V was applied to the surface pad on one end of the energy storage capacitor (highlighted in red), while the opposing terminal and the corresponding ground planes were set to a 0 V reference potential.

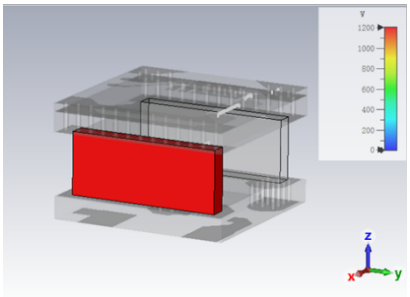

Figure 7. Electrostatic boundary conditions and excitation setup, applying a continuous 1200 V DC voltage to the terminal pad of the storage capacitor

The resulting electric field distribution across the simulated 3D structure is presented in Figure 8. The vector indicates that the electric field lines are primarily concentrated along the vertical interconnecting vias and the

sharp geometric edges of the copper pads. This finding is consistent with the classical tip-discharge effect. The quantitative simulation results indicate that the maximum electric field intensity $E_{\max}$ reaches 14.7 kV/mm.

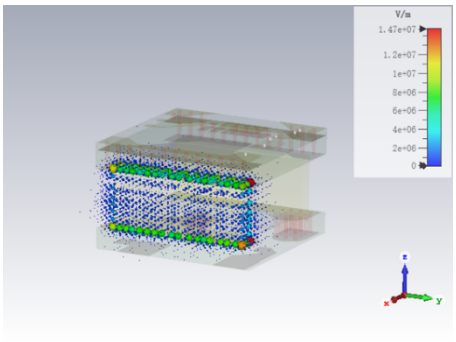

Figure 8. Simulated electric field distribution at 1.2 kV

In light of the high-voltage pulsed operation of the module, there is a possibility for localized heating and long-term insulation degradation. Therefore, a conservative derating strategy was employed. The practical long-term insulation withstand threshold was estimated at 20 kV/mm. Consequently, the simulated maximum field of 14.7 kV/mm ensures an adequate safety margin for reliable operation, thereby preventing premature insulation failure. The localized peak electric field of 14.7 kV/mm is found to remain below the critical breakdown threshold of the surrounding materials, thereby validating the safety margin of the designed layer spacing, via clearance, and overall multi-layer integration strategy against dielectric breakdown under the maximum 1.2 kV operating condition.

Parasitic Parameter Extraction

During the transient discharge phase, the parasitic parameters—specifically the stray inductance and equivalent resistance of the commutation loop—play a dominant role in determining the pulse rise time and the severity of waveform ringing. To quantitatively evaluate these parasitics, a RLC solver was utilized to extract the high-frequency impedance parameters of the multi-layer interconnections.

As delineated in Figure 9, the transient discharge loop is segmented into discrete node pairs for the EM simulation: the capacitor terminals (C+, C-), the MCT solid-state switch terminals (T_A , T_K), and the final pulse output terminals (OUT+, OUT-).

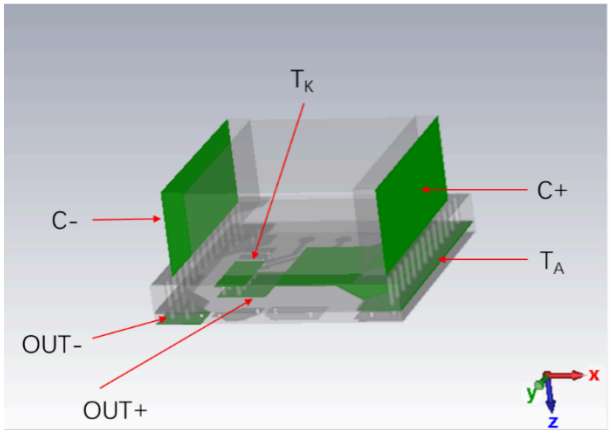

Figure 9. 3D model defining the excitation node pairs for the commutation loop parasitic parameter extraction

The frequency-dependent partial inductance and partial resistance of these critical interconnecting traces were simulated, and the results are plotted in Fig. 10(a) and Fig. 10(b), respectively. As the frequency approaches the MHz range, the skin effect and proximity effect stabilize the impedance values. The simulation results indicate that the partial inductances (L1,1, L2,2, L3,3) are negligible, contributing a cumulative total of approximately 3.15 nH at 1.5 MHz. In a similar manner, the trace resistances (R1,1, R2,2, R3,3) persist at the milliohm level. This low trace impedance is a direct benefit of the proposed vertical 3D stacking structure, which shortens the physical distance between the energy storage capacitor and the solid-state switch compared to a planar PCB layout.

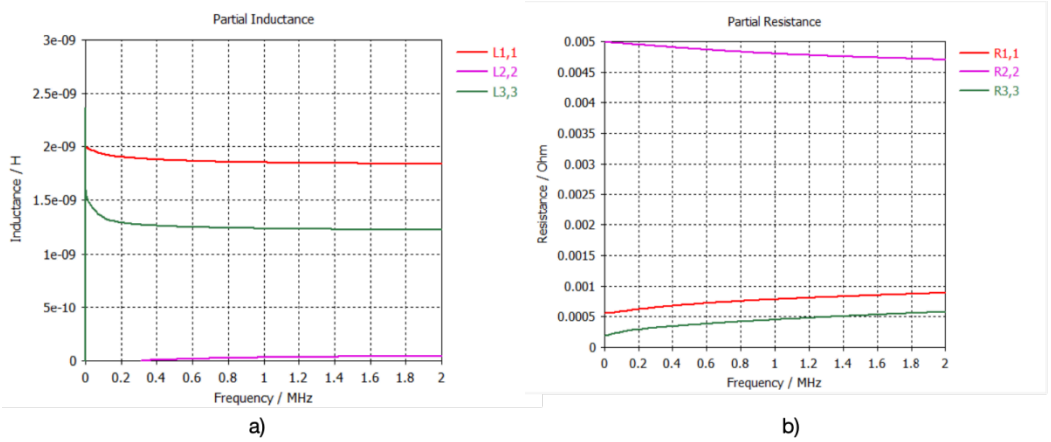

Figure 10. Simulated parasitic parameters of the multi-layer traces versus frequency: (a) partial stray inductance; (b) partial stray resistance

However, the dynamic behavior of the pulse generator is determined by the total loop parameters, which encompass both the layout trace parasitics and the intrinsic parasitics of the discrete components. The simulation results of the PCB traces are combined with the Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR) derived from the component datasheets to summarize the comprehensive series RLC loop parameters, as presented in Table 2.

Table 2. Summary of the Equivalent Series RLC Loop Parameters

Parameter	Symbol	Value	Source / Derivation
Energy Storage Capacitor	C	220 nF	Capacitor Datasheet
Trace Stray Inductance	L_{trace}	3.15 nH	Simulation (@1.5MHz)
Capacitor ESL	L_c	3 nH	Capacitor Datasheet
MCT ESL	L_t	9.2 nH	MCT Datasheet
Simulated load ESL	L_{load}	30 nH	Simulated load parameter
Total Loop Inductance	L_{loop}	45.35 nH	Simulation+Component ESL
Trace Stray Resistance	R_{trace}	6.1 mΩ	Simulation (@1.5MHz)
Capacitor ESR	R_c	7.2 mΩ	Capacitor Datasheet
MCT ESR	R_t	1.8 mΩ	MCT Datasheet
Simulated load ESR	R_{load}	100 mΩ	Simulated load parameter
Total Loop Resistance	R_{loop}	115.1 mΩ	Simulation+Component ESR

Based on the extracted and calculated parameters in Table 2, the complex physical 3D structure can be simplified into an equivalent lumped-parameter circuit model, as illustrated in Fig. 11. The equivalent circuit comprises an ideal pre-charged capacitor C , an ideal high-speed switch, the total lumped loop inductance L_{loop} , and the total loop resistance R_{loop} connected in series with the external load. The fact that the layout trace inductance 3.15 nH accounts for only roughly 7% of the total loop inductance demonstrates that the multi-layer stacking methodology has minimized the spatial parasitic bottleneck, pushing the system's dynamic performance to the limits of the chosen components.

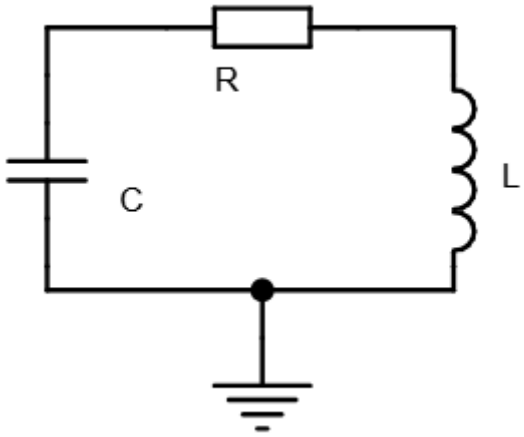

Figure 11. Simplified lumped-parameter equivalent circuit model of pulse discharge loop

To further validate the efficacy of the proposed 3D vertical integration, a comparative simulation was conducted using a conventional planar PCB layout with identical components. As illustrated in Figure 12, three fundamental interconnection segments—namely, capacitor anode to switch anode, switch cathode to load, and load to capacitor cathode—were designated as RLC node pairs for the purpose of extracting the trace parasitics.

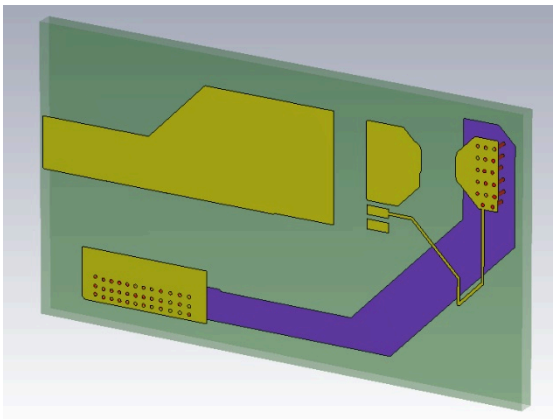

Figure 12. 3D model for planar PCB layout

The comprehensive loop parameters for the planar reference are summarized in Table 3. At an operating frequency of 1.5 MHz, the cumulative trace inductance for the planar layout attained 15.7 nH, which is almost five times higher than the 3.15 nH achieved by the 3D stacked structure.

Table 3. Comparison of equivalent series RLC loop parameters between planar and 3D stacked layouts

Parameter	Symbol	3D Stacked Layout	Planar Layout	Source / Derivation
Trace Stray Inductance	L_{trace}	3.15 nH	15.7 nH	Simulation (@1.5MHz)
Trace Stray Resistance	R_{trace}	6.1 mΩ	8.6 mΩ	Simulation (@1.5MHz)

EXPERIMENTAL SETUP AND RESULTS

Prototype Fabrication

In order to verify the feasibility of the proposed multi-layer integration strategy, a physical prototype of the miniaturized solid-state pulse generator was fabricated and assembled. As illustrated in Figure 13, the custom-designed printed circuit boards (PCBs) corresponding to Layers A, B, D, and F are presented. These FR4-based substrates were prepared for surface-mount component placement or became the framework of the structure.

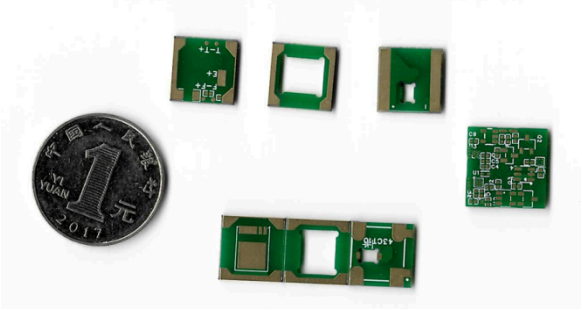

Figure 13. Photograph of the unpopulated customized PCBs corresponding to Layers A, B, D, and F

During the assembly phase, the individual planar layers and the bulky core components (i.e., the capacitor and the transformer) were stacked using a soldering process. A critical physical challenge in this 3D architecture is establishing reliable electrical interconnections across the vertical stack. This is particularly challenging because it involves routing the high-voltage sampling feedback and the trigger signals from the top interface (Layer A) down to the bottom control circuitry (Layer F).

In order to address this issue without compromising the integrity of the internal high-voltage insulation barriers or increasing the structural volume, external lateral wiring was employed. Flexible, silicone-insulated wires were routed and soldered along the lateral sidewalls of the stacked module. It is important to note that both of these signals are 12V low-voltage signals. In contrast, high-voltage energy transmission—including

flyback boost and energy storage capacitor discharge—is transmitted via interlayer vias or a stacked interconnect structure. The implementation of corresponding PCB frames within Layers C and E would facilitate the identification of the four wires within the confines of the PCB frames. However, this approach would concomitantly result in a substantial augmentation of the complexity inherent to the soldering process. The fully assembled prototype is presented in Figure 14. The integrated module's physical dimensions are precisely $15.0 \times 15.0 \times 15.7\,\mathrm{mm}^3$, thereby evidencing its remarkably compact form factor and its capacity for high-density packaging, which is facilitated by the proposed multi-layer stacking methodology.

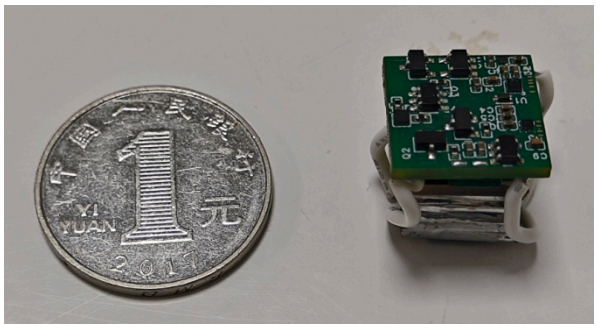

Figure 14. Photograph of the assembled miniaturized solid-state pulse generator prototype, illustrating the vertical stacking structure and the lateral silicone wire interconnections

Experimental Testbench and Steady-State Boost Performance

An experimental testbench was established for the purpose of evaluating the electrical characteristics of the assembled prototype, as illustrated in Figure 15. The prototype is powered by the DC power supplies (Aglient E3632A and WANPTEK WPS305H) that is routed through a custom-designed power conversion and host development board. This auxiliary board fulfills dual functions: it both regulates the low-voltage input and provides the timed pulse-width modulation (PWM) driving pulses and trigger signals necessary for the module's operation. The transient electrical signals are captured using a digital oscilloscope (Tektronix TBS2104B) equipped with a high-voltage differential probe (PINTEON PT-5240). Furthermore, the Rogowski coil (PINTEON DK-14400) has been incorporated into the testbed to measure the high di/dt transient current during the pulse discharge phase.

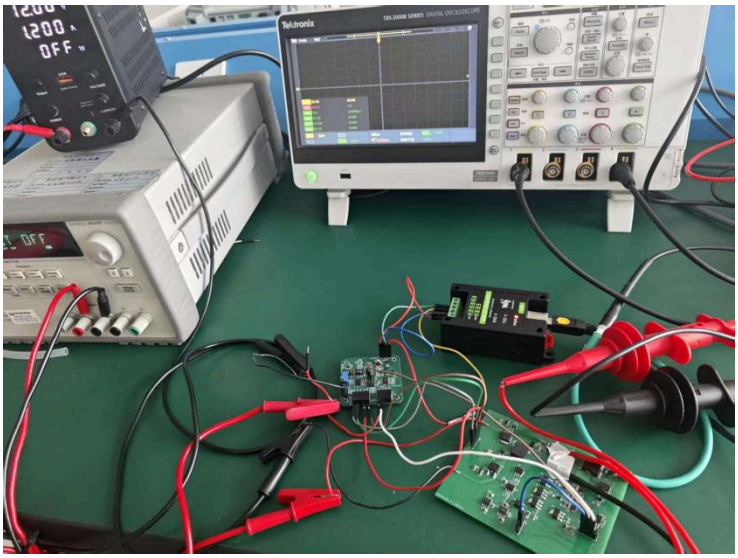

Figure 15. Experimental testbench setup

An evaluation of the steady-state boost capability of the miniaturized flyback converter was conducted. The charging voltage waveform across the 220 nF energy storage capacitor was continuously monitored, and the result is illustrated in Figure 16.

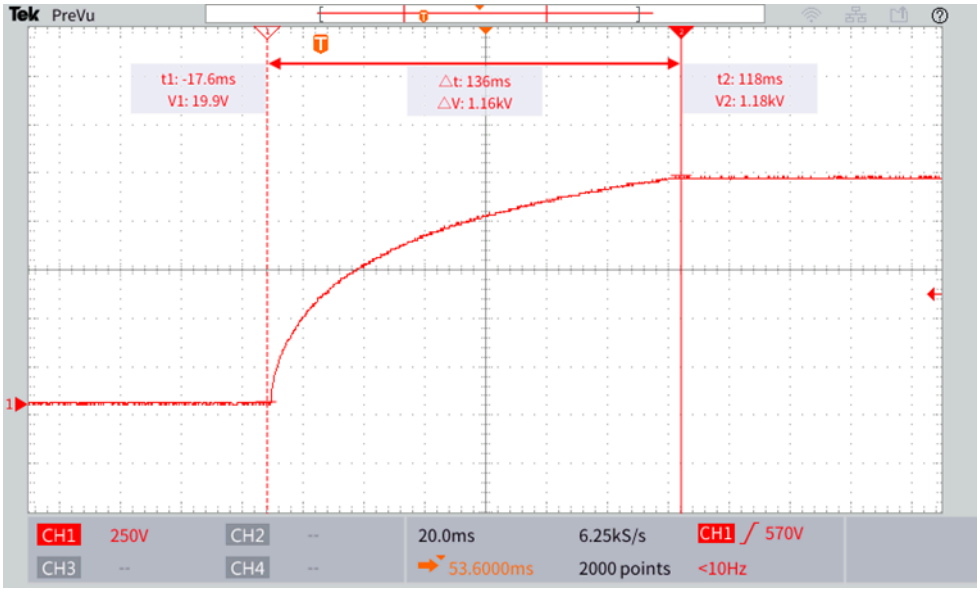

Figure 16. Oscilloscope waveform of the steady-state boost phase

Upon the activation of the primary-side PWM signal, the LTCC transformer and the embedded rectifying diode initiate the pumping of magnetic energy into the capacitor in a sequential manner. As indicated by the cursor measurements on the oscilloscope, the capacitor voltage smoothly rises from the baseline to a target high

voltage of approximately 1.18 kV. The total charging time required to reach this predetermined voltage level is 136 milliseconds. The charging trajectory manifests the functionality of the high-density step-up stage, unmarred by phenomena such as magnetic saturation or insulation breakdown. Additionally, as the voltage approaches 1.20 kV, the voltage profile exhibits a flattening trend, suggesting the engagement of the high-voltage sampling network and the Pulse Skipping Modulation (PSM) control loop, which are situated on Layer F. The PSM strategy has been demonstrated to maintain the target voltage level with efficiency, compensating for component leakage and preventing dangerous overcharging. As a result, the module is fully prepared for the subsequent solid-state discharge sequence.

Pulse Output Characteristics

The transient discharge capability of the miniaturized module was evaluated through the implementation of a low-impedance short-circuit discharge test. Subsequent to the steady-state boost phase, the 220-nF capacitor was pre-charged to 1.2 kV. Upon receiving a synchronized external trigger signal at the Layer A interface, the embedded MCT (Layer B) rapidly transitioned into the conduction state, releasing the stored energy. The transient discharge current was captured using the Rogowski coil, and the corresponding waveform is presented in Figure 17.

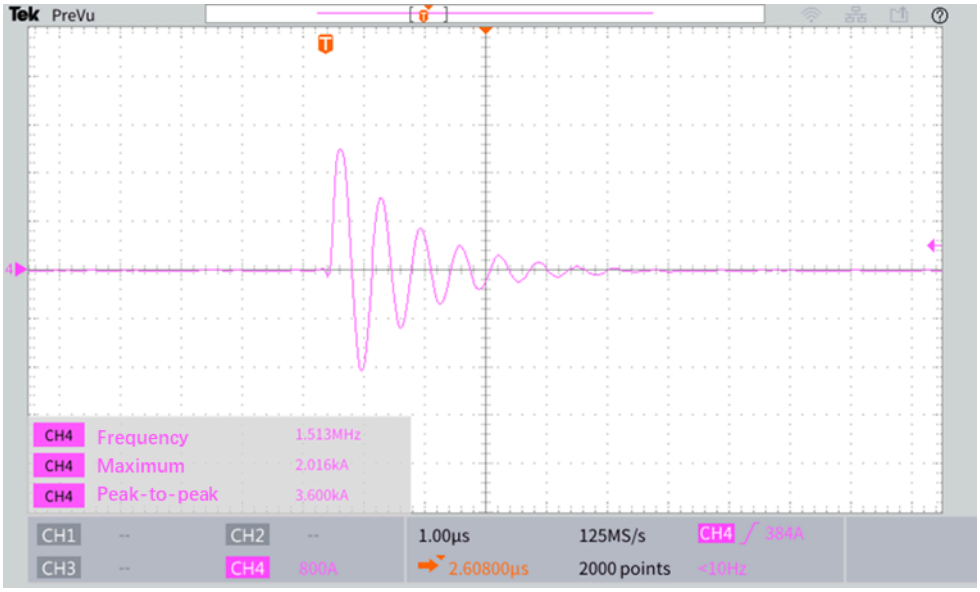

Figure 17. Oscilloscope waveform of the transient pulse discharge current

As demonstrated in Figure 17, the discharge current displays a standard underdamped sinusoidal oscillation, which is indicative of an RLC discharge loop with low equivalent series resistance (ESR). The measured

peak discharge current I_{peak} attains a remarkable value of 2.016 kA, with a peak-to-peak value of 3.600 kA. This extreme current surge confirms that the compact MCT switch and the vertical interconnections can safely handle kilo-ampere-level pulses, operating well within the MCT's maximum 4 kA rating. Furthermore, the negative half-cycle of the oscillating current demonstrates the role of the MCT's built-in anti-parallel freewheeling diode, which provides a conduction path for the reverse current. This, in turn, protects the solid-state switch from reverse overvoltage breakdown.

DISCUSSION

A performance comparison of the proposed 3D-stacked miniaturized pulse generator with other recently reported solid-state pulse generators is summarized in Table 4. This comparison is intended to evaluate the advancements of the proposed pulse generator.

Table 4. Comparison of the Proposed Pulse Generator with Existing Literature

Specifications	[23]	[24]	Proposed Work
Application	rTMS (Biomedical)	DBD Plasma Jets	Compact Systems
Main Switch Type	IGBT	IGBT	Integrated MCT
Max Output Voltage	1.2 kV	6 kV	1.2 kV
Peak Current	700 A	Not Specified	2.016 kA
Required Input Source	External HV DC Supply	220V/50Hz AC	Low-Voltage DC Input (12V)
Integrated Step-up	No	Yes	Yes (Flyback with LTCC)
Dimensions (mm)	114.2×120.6×55	105×260×180	15.0×15.0×15.7
Total Volume	757.6cm³	4914cm³	3.533cm³

As illustrated in Table 4, while existing pulse generators demonstrate commendable electrical characteristics for their designated applications, they encounter substantial constraints with regard to volume and system integration.

The proposed integrated pulse generator consolidates the complete process of energy conversion, storage, and rapid discharge into a volume of 3.533cm³.

CONCLUSION

While the proposed $15 \times 15 \times 15.7\,\mathrm{mm}^3$ prototype demonstrates the physical feasibility and electrical superiority of the multi-layer stacking methodology for nanosecond pulse generation, there remains significant potential for further structural and operational optimization.

First, future iterations will transition from the current FR4-based discrete board stack to a monolithic low-temperature cofired ceramic (LTCC) housing. Leveraging advanced LTCC fabrication processes will allow us to eliminate the external lateral silicone wires that are currently used to interconnect the top-layer high-voltage feedback and bottom-layer trigger signals. Conversely, we will employ the approach of directly co-firing internal vertical interconnections, such as embedded conductive vias, within the ceramic substrate. This transition will eliminate the manual wiring process and create a true 3D system-in-package (SiP) architecture. This transition is expected to result in several key benefits, including the maximization of volumetric power density, the enhancement of electromagnetic shielding, and the improvement of the thermo-mechanical reliability of the module. These advancements are crucial for ensuring the durability of the module in industrial manufacturing environments and for facilitating integration into plasma applicators. This integration is paramount for the on-demand surface modification of delicate fabrics and leathers. However, it is important to note that the experimental validation in this study was conducted under near short-circuit conditions to characterize the maximum energy delivery and pulse waveforms of the generator. In practical textile and leather processing applications, nonlinear plasma loads will be involved. Given the considerable heterogeneity inherent in industrial plasma treatment heads, the development of a dedicated, miniaturized plasma load designed to match the compact scale of this generator is imperative. Subsequent research endeavors will thus concentrate on the structural design of this miniaturized plasma head and the subsequent industrial validation of the complete integrated system under realistic, nonlinear load conditions.

Second, subsequent research endeavors will seek to expand this stacked architecture to operate at significantly higher voltage regimes by leveraging established multi-layer integration principles. However, achieving compact integration at elevated voltages will inevitably intensify the dielectric stress. Consequently, subsequent research will explore sophisticated internal electric field grading methodologies, innovative high-dielectric-strength encapsulants, and cascading ultra-compact solid-state switching stages to safely manage extreme electric fields within micro-volumes. Realizing higher voltage outputs within miniaturized footprints will ultimately unlock new capabilities in textile and leather engineering. This includes achieving deeper non-thermal plasma penetration for thick leather hides, facilitating high-throughput, continuous, roll-to-roll fabric treatments, and enabling more aggressive electro-pulse cottonization of natural fibers. This will drive the industry toward greener, more efficient processing paradigms.

Author Contributions

All work in this manuscript was independently completed by Quanlin Li.

All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest

The author declares no conflict of interest.

Funding

This research received no external funding.

Acknowledgements

Not applicable.

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